SPECIFICATION AMENDMENTS

At page 1, lines 1-2, please amend the Title as follows:

~~MICROPROCESSOR WITH HARDWARE CONTROLLED POWER MANAGEMENT~~ INSTRUCTION-INITIATED POWER MANAGEMENT METHOD FOR A PIPELINED DATA PROCESSOR

At page 1, between lines 2 and 3, please insert the following:

RELATED APPLICATIONS

This is a division of U.S. patent application no. 10/216,615, filed August 9, 2002.

At page 1, lines 4-6, please amend the text of the section entitled "Technical Field of the Invention" as follows:

This invention relates in general to integrated circuits, and more particularly to a ~~microprocessor having hardware controlled~~ pipelined data processor with power management control.

At page 4, lines 3-21, please amend the text of the section entitled "Summary of the Invention" as follows:

~~In accordance with the present invention, a method and apparatus is provided which provides significant advantages in reducing the power consumption of a microprocessor.~~

~~In the present invention, a processing unit includes a plurality of subcircuits and circuitry for generating a clock signal thereto. Circuitry is provided for detecting the assertion of a control signal; responsive to the control signal, disabling circuitry disables the clock signal to one or more of the subcircuits.~~

~~The present invention provides significant advantages over the prior art. A significant reduction in the power consumed by a computer may be effected by disabling the clock to the microprocessor circuitry. The present invention allows the disabling and enabling of the microprocessor clock signals to be controlled by a single control signal. Further, an acknowledge signal may be provided to notify external circuitry of the suspended state of the microprocessor.~~

In accordance with the presently claimed invention, an instruction-initiated power management method for a pipelined data processor is provided by which a clock signal to pipeline subcircuitry is selectively disabled in response to an instruction executed by the pipeline subcircuitry.

In accordance with one embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having active and inactive states, on one or more of the plurality of incoming instructions for data processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to the active first clock signal, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions, and

executing, with a second portion of the pipeline subcircuitry in response to the active first clock signal, the one or more decoded instructions;

generating, in response to the one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states

including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals with the second selected assertion and de-assertion states following reception of the power management instruction; and

generating, in response to the one or more clock control signals, at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals.

In accordance with one embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having active and inactive states, on one or more of the plurality of incoming instructions for data processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to the active first clock signal, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions, and

executing, with a second portion of the pipeline subcircuitry in response to the active first clock signal, the one or more decoded instructions;

generating, in response to the one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more

local control signals; and

generating, in response to the one or more clock control signals, at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals and following reception of the power management instruction.

In accordance with one embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles, on one or more of the plurality of incoming instructions for data processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to at least a first one of the plurality of first clock signal cycles, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions, and

executing, with a second portion of the pipeline subcircuitry in response to at least a second one subsequent to the first one of the plurality of first clock signal cycles, the one or more decoded instructions;

generating, in response to the one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals with the second selected assertion and de-assertion states following reception of the power management instruction; and

generating, in response to the one or more clock control signals, at least the first clock signal with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals.

In accordance with one embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles, on one or more of the plurality of incoming instructions for data processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to at least a first one of the plurality of first clock signal cycles, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions, and

executing, with a second portion of the pipeline subcircuitry in response to at least a second one subsequent to the first one of the plurality of first clock signal cycles, the one or more decoded instructions;

generating, in response to the one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals; and

generating, in response to the one or more clock control signals, at least the first clock signal with the first clock signal inactive state corresponding to the one or

more second selected assertion and de-assertion states of the one or more clock control signals and following reception of the power management instruction.

In accordance with one embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having active and inactive states, on one or more of the plurality of incoming instructions for data processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to the active first clock signal, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions, and

executing, with a second portion of the pipeline subcircuitry in response to the active first clock signal, the one or more decoded instructions;

generating, in response to the first clock signal, a second clock signal and the one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals with the second selected assertion and de-assertion states following reception of the power management instruction; and

generating, in response to the one or more clock control signals, the first and second clock signals with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock

control signals and the second clock signal having active and inactive states substantially independent of the one or more second selected assertion and de-assertion states of the one or more clock control signals.

In accordance with one embodiment of the presently claimed invention, a method for processing electronic data includes:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having active and inactive states, on one or more of the plurality of incoming instructions for data processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to the power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to the active first clock signal, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of the one or more of the plurality of incoming instructions, and

executing, with a second portion of the pipeline subcircuitry in response to the active first clock signal, the one or more decoded instructions;

generating, in response to the first clock signal, a second clock signal and the one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to the one or more first selected assertion and de-assertion states of the one or more local control signals; and

generating, in response to the one or more clock control signals, the first and second clock signals with the first clock signal inactive state corresponding to the one or more second selected assertion and de-assertion states of the one or more clock control signals and following reception of the power management instruction, and

with the second clock signal having active and inactive states substantially independent of the one or more second selected assertion and de-assertion states of the one or more clock control signals.

At page 19, lines 3-8, please amend the text of the section entitled "Abstract of the Disclosure" as follows:

~~A processing unit includes a plurality of subcircuits and circuitry for generating clock signals thereto. Detection circuitry detects the assertion of a control signal and disabling circuitry is operable to disable the clock signals to one or more of the subcircuits responsive to the control signal.~~ An instruction-initiated power management method for a pipelined data processor by which a clock signal to pipeline subcircuitry is selectively disabled in response to an instruction executed by the pipeline subcircuitry.